REMARKS

Reconsideration of this application is respectfully requested in view of the following remarks.

Claims 1, 4-8 and 10-20 are currently pending in the application and subject to examination.

A Pre-Appeal Brief Request for Review was filed in this application on September 21, 2007. The Notice of Panel Decision resulting from that Review indicated that the previous rejection was withdrawn, and that a new Office Action would be issued.

Notwithstanding the above, in the outstanding Office Action, the Examiner again rejected claims 1, 4-8, 10-13 and 20 under U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,452,004 to Roberts, (hereinafter, "Roberts"); claims 14-16 under 35 U.S.C. § 103(a) as being unpatentable over Roberts in view of U.S. Patent No. 4,827,348 to Ernest et al. (hereinafter, "Ernest"); and claims 17-19 under 35 U.S.C. § 103(a) as being unpatentable over Roberts in view of Ernest and further in view of U.S. Patent No. 5,382,974 to Soeda et al. (hereinafter, "Soeda"). The Applicant hereby traverses the rejections, as follows.

In making the rejections of claims 1 and 14, the Examiner asserts that Roberts discloses "a plurality of reset signal lines (Fig. 2, element 68) disposed along the row direction, each being associated with one pixel row for supplying a reset signal (col. 8, lines 44-55; col. 7, lines 11-26)..." and "an overall reset controller (Fig. 1, element 208; col. 12, lines 28-50) supplying an overall reset signal to all of said reset signal lines at a time..." *Office Action*, p. 3.

According to Roberts, element 68 of Fig. 2 is a "gate 68 of a FET 70." Col. 7, lines 11-26 of Roberts describe an operation in which one of two selected pixels is reset. Col. 8, lines 44-55 of Roberts describe an operation with respect to Fig. 8 in which a pixel 40 is reset. Element 208 shown in Fig. 1 of Roberts is a control cache that performs a buffer memory function (see col. 13, line 30 of Roberts). The Applicant submits that neither the cited portions of Roberts, nor any other portion thereof, discloses or suggests at least the features of a plurality of reset signal lines disposed along the row direction, each being associated with one pixel row for supplying a reset signal; and an overall reset controller for supplying an overall reset signal to all of said reset signal lines at one time, as recited in independent claims 1 and 14. Therefore, the Applicant requests the Examiner to point out specifically where such a teaching may be found in Roberts.

The Examiner further asserts that Roberts discloses "(a) a photoelectric converter element having a cathode (Fig. 9, element 42) and (b) a switching circuit (Fig. 9, element 40) electrically connected to the photoelectric converter element for controlling generation of an output signal representing electric charge accumulated in the photoelectric converter element and discharge of the electric charge (col. 8, line 44-55)." *Id.*

However, there is no element 42 or 40 of Fig. 9. Element 42' of Fig. 9 is a photodiode, and element 40' of Fig. 9 is a pixel. Element 40' of Fig. 9 is not a switching circuit electrically connected to the photoelectric converter element for controlling generation of an output signal representing electric charge accumulated in

the photoelectric converter element and discharge of the electric charge, as recited in independent claims 1 and 14.

Further, in making the rejection of claims 1 and 14, the Examiner asserts that "Roberts discloses that the row selection and reset functions are implemented in a conventional row-by-row order. See column 7, lines 10-47." *Office Action*, page 4, lines 4-5. However, at col. 7, lines 10-47, Roberts discloses that the photodiodes of the pixels would saturate their charge storage capacitors if this scan is conducted in the conventional row by row order. The Applicant does not find a teaching in Roberts for performing the row selection and reset functions in row by row order.

In the outstanding Office Action, the Examiner admits that Roberts fails to disclose that the row shift circuit operates without a random access function, but asserts that the row shift circuit "having no random access function" is considered a negative claim limitation. The Applicant submits that the total recitation of the portion of claim 1 in question, i.e., "a row shift circuit including a row read scan circuit capable of supplying a read signal to said plurality of row selection signal lines sequentially, the row shift circuit having no random access function" recites a row shift circuit having the specified structure and having no random access function and, therefore, is not a negative limitation.

Also, in the outstanding Office Action, the Examiner further asserts "Roberts teaches a more complicated circuit which includes a random access circuit. The elimination of this feature from the circuit of Roberts would provide a row shift circuit that does not operate using a random access function. The elimination of this feature would further, result in a simplified row shift circuit..." The Applicant submits that there is no

support in Roberts for this allegation. As explained above, Roberts describes that if the scan is conducted in the conventional row by row order, the capacitor will be saturated. As such, Roberts appears to teach away from the Examiner's assumption that removing the random access function therefrom would result in a simplified circuit. Moreover, if the capacitor will be saturated if the scan is conducted in the conventional row by row order, as taught by Roberts, one would not be motivated to make the modification as suggested by the Examiner.

It is noted that Ernest does not cure the deficiencies of Roberts noted above. Moreover, Soeda is not cited for and does not cure the deficiencies of the combination of Roberts and Ernest.

For all of the above reasons, the Applicant submits that independent claims 1 and 14 are allowable over Roberts. As claims 1 and 14 are allowable, the Applicant submits that claims 4-8 and 10-13, and claims 15-19, which depend from allowable claims 1 and 14, respectively, are likewise allowable for at least the reasons set forth above with respect to claims 1 and 14.

The Applicant further submits that claim 20 is similarly allowable.

CONCLUSION

For all of the above reasons, it is respectfully submitted that claims 1, 4-8 and 10-20 are in condition for allowance and the issuance of a Notice of Allowability is earnestly solicited.

Should the Examiner determine that any further action is necessary to place this application into better form, the Examiner is encouraged to telephone the undersigned representative at the number listed below.

In the event this paper is not considered to be timely filed, the Applicant hereby petitions for an appropriate extension of time. The Commissioner is hereby authorized to charge any fee deficiency or credit any overpayment associated with this communication to Deposit Account No. 01-2300, referencing docket number **107317-00026.**

Respectfully submitted,

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